CLAIMS

What is claimed is:

1. A Doherty amplifier system comprising:

an input splitter for splitting an input signal into first and second potions;

first and second signal paths for carrying respectively the first and second portions of the input signal;

one or more input phase shifters for realizing a net relative phase shift of approximately 90° between signals carried on the first and second signal paths;

a carrier amplifier having an output situated along a selected one of the first and second paths;

a peaking amplifier having an output situated along one of the first and second paths other than the selected one; and

a quarter wave transformer/combiner circuit coupled directly to the outputs of the carrier and peaking amplifiers for realizing a net relative phase shift of approximately 90° between the amplifier outputs so the two are approximately in-phase, and combining the two to form one or more output signals.

2. The system of claim 1, wherein the carrier and peaking amplifiers comprise bipolar junction transistors.

3. The system of claim 1, wherein the carrier and peaking amplifiers comprise field effect transistors.

4. The system of claim 1, wherein the quarter wave transformer/combiner circuit comprises a lumped pi network having an integral number of sections coupled in parallel, each section comprising a series combination of a shunt inductance, series capacitance, and shunt inductance.

5. The system of claim 4, wherein the shunt inductances absorb bond wire parasitics and supply DC bias current to the carrier and peaking amplifiers.

6. The system of claim 4 wherein the series capacitances are integrated directly on an RFIC.

7. The system of claim 4 where the shunt inductances are realized using bond wires of an RFIC.

8. The system of claim 1 further comprising a matching circuit coupled to the one or more outputs of the quarter wave transformer/combiner circuit for transforming the output impedance of the quarter wave transformer/combiner circuit to a desired impedance.

9. The system of claim 1 wherein the quarter wave transformer/combiner circuit is configured to decrease the load impedance to the carrier amplifier as the input power increases.

10. A Doherty amplifier system comprising:

means for splitting an input signal into first and second potions;

first and second signal path means for carrying respectively the first and second portions of the input signal;

phase shifting means for realizing a net relative phase shift of approximately 90° between signals carried on the first and second signal path means;

carrier amplifier means having an output for amplifying a signal carried by a selected one of the first and second path means;

peaking amplifier means having an output for amplifying a signal carried by one of the first and second path means other than the selected one; and

quarter wave transformer/combiner means coupled directly to the outputs of the carrier and peaking amplifier means for realizing a net relative phase shift of approximately 90° between the amplifier means outputs so the two are approximately in-phase, and combining the two to form one or more output signals.

11. A quarter wave transformer/combiner circuit comprising a lumped pi network having an integral number n of sections coupled in parallel, where n is an integer greater than 1, each section comprising the series combination of a first shunt inductance, a series capacitance, and a second shunt inductance.

12. The circuit of claim 11 wherein each of the sections has a point intermediate between the first shunt inductance and the series capacitance for coupling to the output of a carrier amplifier output.

13. The circuit of claim 12 wherein each of sections has a point intermediate between the series capacitance and the second shunt inductance for coupling to a peaking amplifier output.

14. The circuit of claim 13 wherein each of the sections has a point intermediate between the series capacitance and the second shunt inductance for coupling to a summing node.

15. The circuit of claim 12 wherein the opposing end of the first shunt inductance in each section is coupled to a power supply voltage configured to provide a bias voltage to the carrier amplifier.

16. The circuit of claim 13 wherein the opposing end of the second shunt inductance in each section is coupled to a power supply voltage configured to provide a bias voltage to the peaking amplifier.

17. The system of claim 1 implemented as an RF integrated circuit.

18. The system of claim 1 implemented with solid state components.